

09/991,164
Attorney Docket: 42390.P12570

Remarks

Applicant notes with appreciation the indication that Claims 11-26 and 31-42 are allowed, and that Claims 2 and 9-10 are directed toward allowable subject matter. Reconsideration of the above referenced application in view of the enclosed remarks is requested. No Claims are currently amended. Claims 1 to 42 are now pending in the application.

ARGUMENT

Claims 1, 3-8 and 27-30 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,624,962 to Kodama et al. (hereinafter "Kodama et al."). This rejection is respectfully traversed and Claims 1, 3-8 and 27-30 are believed allowable based on the following discussion.

As for Claims 1 and 27, the Examiner asserts that Kodama et al. discloses a system to *determine a power state of a non-volatile storage device; and selectively buffer a file system write request relating to the non-volatile storage device based on the determined power state of the non-volatile storage device*. This assertion is in error.

Kodama et al. discloses a system for avoiding read/write errors when accessing a storage device during non-ordinary power states or the transition to/from ordinary mode. When a storage device is not fully spun-up because it is in power save mode or transitioning to/from power save there may be read/write errors resulting from the head not being on track. Kodama et al. solves this problem by identifying the power mode of the storage device. If the power mode is not ordinary mode, Kodama et al. teaches accessing the storage device twice. In some cases, dummy data is written first. By performing an extra access (either dummy write or seek access, or other command), the storage device will likely be fully spun-up (powered on in ordinary mode) by the time the requested access, or write, is actually performed. At no time does Kodama et al. teach buffering the data for a later time.

In contrast, Applicant's claimed invention requires that a *write operation is buffered to physical memory* (Claim 1) or *selectively buffering a file system write request relating to the non-*

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volatile storage device based on the determined power state of the non-volatile storage device (Claim 27). Applicant's claimed invention determines the power state of a storage device, but does not force the device to power up to ordinary mode and then write to it, as taught by Kodama et al. Instead, when the claimed device determines that the power state is not in ordinary mode (or powered up), the write data is buffered to physical memory until such time as the storage device becomes available. If the teachings of Kodama et al. are applied to Applicant's invention, buffering would not be permitted. Instead, the non-volatile storage device would be forced to be powered up and written to immediately. Thus, Claims 1 and 27 and their progeny are believed allowable.

With respect to Claims 6 and 29, the Examiner asserts that Kodama et al. teach *writing one or more buffered write operations to the device upon an occurrence of a predetermined condition*. This assertion is incorrect. At Col. 7, lines 49-62, as cited by the Examiner, Kodama et al. teach that a dummy read/write operation is performed before the requested read/write operation. At no time do Kodama et al. teach buffering a read/write operation. Delaying an operation is not the same as buffering an operation. It should be apparent to one of ordinary skill in the art that buffering implies storing the operation in a separate location for later access. Delaying an operation is typically performed merely by inserting an intervening operation. No buffering is necessary for a delay. Nor do Kodama et al. teach or suggest that the read/write operation is to be buffered, but only delayed. Further, the system of Kodama et al. requires that the mode be immediately switched to power on mode after receiving a read/write request, and does not allow for buffering and later access.

With respect to Claim 7, the Examiner asserts that Kodama et al. teach waiting a predetermined amount of time before writing one or more buffered write operations to the device. This claim is distinguishable from the cited reference because Kodama et al. do not teach buffering the data. Further Kodama et al. teach only waiting a predetermined time before writing to a storage device *after* powering the system up. The time interval is predetermined, and likely hard-coded into the device. This is not the same as detecting a predetermined condition of a predetermined time elapsing.

With respect to Claim 8, the Examiner asserts that Kodama et al. teach receiving user input relating to one or more predetermined conditions. The cited reference is improper (Col. 1,

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lines 17-30) as it describes a "command received from a host." One of ordinary skill in the art will appreciate that the host is a computing device and commands received from the host are often automatically generated without user interaction. Kodama et al. do not teach or suggest receiving user (human) input relating to the predetermined conditions.

Claim 28 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kodama et al. in view of U.S. Pat. No. 6,412,045 to DeKoning et al. (hereinafter "DeKoning et al."). This rejection is respectfully traversed and Claim 28 is believed allowable based on the foregoing and following discussion.

Applicant has discussed the teachings of DeKoning et al. in the previous response, and reinstates these arguments. Specifically, DeKoning et al. teach determining whether cache batteries are operational, i.e., whether caching may take place without fear of data loss, but do not teach determining whether the host computer is operating under AC or DC (battery) power. DeKoning et al. merely teach whether an operational battery is present. In addition, as discussed above, Kodama et al. do not teach or suggest buffering a write request. Kodama et al. merely teach inserting intervening accesses to delay the write requests. Kodama et al. require that the storage device be powered up immediately after receiving a write request and do not allow for later write operations after buffering. Thus, combining the teachings of Kodama et al. with DeKoning et al. will not result in Applicant's claimed invention. All claims remaining in the application are now allowable.

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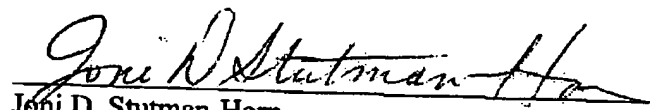
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CONCLUSION

In view of the foregoing, Claims 1 to 42 are all in condition for allowance. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (703) 633-6845. Early issuance of Notice of Allowance is respectfully requested. Please charge any shortage of fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such account.

Respectfully submitted,

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